

What is claimed is:

1       **1.**       A system for driving an optoelectronic device, comprising:  
2       a buffer circuit for receiving a differential electrical signal;  
3       a dedicated voltage regulator having an input adapted to receive a control  
4 signal and an output adapted to provide an output voltage that is a function of  
5 the control signal; and  
6       a driver amplifier having a first input coupled to the output of said buffer  
7 circuit and a second input coupled to said voltage regulator and an output for  
8 providing a precisely controlled waveform to an optoelectronic device.

1       **2.**       A system as in claim 1, wherein said buffer circuit comprises:  
2       an attenuating input stage having a pair of resistors; and  
3       an amplifying output stage.

1       **3.**       A system as in claim 1, wherein said buffer circuit comprises:  
2       an attenuating input stage having a pair of resistors; and  
3       an amplifying output stage; and  
4       said driver amplifier comprises:  
5       first and second amplifying transistors adapted to receive a differential  
6 input at their respective base regions; and  
7       first and second load resistors connected between the respective  
8 collector regions of said first and second transistors and the dedicated voltage  
9 regulator;  
10       a common connection of the collector region of said second transistor and  
11 said second load resistor adapted to provide an output to an optoelectronic  
12 device.

1       **4.**       A system as in claim 1, wherein said driver amplifier comprises:  
2       first and second amplifying transistors adapted to receive a differential  
3 input at their respective base regions; and  
4       first and second load resistors connected between the respective  
5 collector regions of said first and second transistors and the dedicated voltage  
6 regulator;

7 a common connection of the collector region of said second transistor and  
8 said second load resistor adapted to provide an output to an optoelectronic  
9 device.

1 5. A system as in claim 4, wherein the emitters of said first and  
2 second transistors are connected to form a common node, and further  
3 comprising:

4 a third transistor connected between said common node and ground.

1 6. A system as in claim 4 further comprising:

2 a capacitor connected between said output voltage and ground.

1 7. A system as in claim 4, further comprising:

2 a compensation load connected coupled between the collector region of  
3 said first transistor and ground.

1 8. A system as in claim 7, further comprising:

2 a capacitor connected between said output voltage and ground.

1 9. A system as in claim 7, wherein said compensation load  
2 comprises:

3 a resistor; and

4 at least one diode connected in series with said resistor.

1 10. A system as in claim 1, further comprising:

2 a laser diode.

1 11. A system as in claim 10, wherein said laser diode is a VCSEL.

1 12. A system as in claim 1 further comprising:

2 an additional buffer circuit for receiving a differential electrical  
3 signal;

4 an additional dedicated voltage regulator having an input adapted  
5 to receive a control signal and an output adapted to provide an output voltage  
6 that is a function of the control signal; and

7 an additional driver amplifier having a first input coupled to the  
8 output of said additional buffer circuit and a second input coupled to said

9 additional voltage regulator and an output for providing a precisely controlled  
10 waveform to an additional optoelectronic device.

1       **13.** A system as in claim 12, wherein said optoelectronic device and  
2 said additional optoelectronic device are light emitting diodes formed as an  
3 integrated array.

1       **14.** A system as in claim 13, wherein said integrated array comprises:  
2 VCSEL's.

1       **15.** A system as in claim 13 wherein said light emitting diodes have their  
2 cathodes connected in common and to ground.

1       **16.** A system as in claim 1, wherein said driver amplifier comprises:  
2 a first amplifier having first and second differentially connected  
3 transistors and a first current source;  
4 a second amplifier having third and fourth differentially connected  
5 transistors and a second current source; and  
6 a time delay network connected between the inputs of said first and  
7 second amplifiers.

1       **17.** A system as in claim 16 wherein a first input is coupled to the base of  
2 the first and third transistors and a second input is coupled to the base of the  
3 second and fourth transistors.

1       **18.** A system as in Claim 17 wherein the collector of the first transistor is  
2 connected to the collector of the fourth transistor and the collector of the  
3 second transistor is connected to the collector of the third transistor.

1       **19.** A system as in claim 1, wherein said driver amplifier comprises:  
2 first and second amplifying transistors adapted to receive a differential  
3 input at their respective base regions, the emitters of said first and second  
4 transistors being connected to form a common node;  
5 first and second load resistors connected between the respective  
6 collector regions of said first and second transistors and the dedicated voltage  
7 regulator;

8           a common connection of the collector region of said second transistor and  
9       said second load resistor adapted to provide an output to an optoelectronic  
10     device.

11           a third transistor connected between said common node and ground;  
12           said dedicated voltage regulator has an output transistor;

13           a fourth transistor connected to said output transistor forming a first  
14     current mirror; and

15           a fifth transistor connected to said third transistor forming a second  
16     current mirror.

1           **20.** A system as in claim 19, further comprising:

2           sixth and seventh transistors forming a third current mirror; and

3           a third resistor connected to said seventh transistor.

1           **21.** A system as in claim 20, further comprising:

2           a comparator connected to the common connection of said third resistor  
3     and said seventh transistor.

1           **22.** A method of supplying a channel specific voltage to each one of a  
2     plurality of common cathode connected diodes in a laser diode array,  
3     comprising the steps of:

4           buffering first and second differential electrical input signals and providing  
5     first and second buffered differential electrical output signals to first and second  
6     differential amplifiers;

7           generating first and second regulated voltages in response to first and  
8     second control signals;

9           supplying the first regulated voltage and the first buffered electrical  
10    output signal to a first driver amplifier adapted to supply a drive voltage to the  
11    anode of a first one of the plurality of common cathode connected diodes; and  
12           supplying the second regulated voltage and the second buffered electrical  
13    output signal to a second driver amplifier adapted to supply a drive voltage to  
14    the anode of a second one of the plurality of common cathode connected  
15    diodes.